ABSTRACT OF THE DISCLOSURE

A digital matched filter includes a received signal holding unit for holding received signal samples, a spreading code generating unit for generating known spreading codes, and a correlation value calculating unit for calculating a correlation value between the received signal samples and the spreading codes. The received signal holding unit is formed of a plurality of registers arranged in parallel and gate circuits are provided at respective preceding stages for masking signal input unless signal writing is to be performed. The correlation value calculating unit is formed of a plurality of slow-operation calculating circuits arranged in parallel. Each calculating circuit is divided into product-sum calculating units at the anterior and posterior stages respectively. The product-sum calculating unit at the posterior stage is stopped when it is not the time of detecting a peak value in order to reduce power consumption.